NEWS RELEASE

SmartDV™

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SmartDV Unveils Automation Tool Suite for Use with
Its Extensive Verification IP Portfolio
Improves Productivity, Eliminates Tedious, Error-Prone Manual Effort

SAN JOSE, CALIF. — May 4, 2021 — SmartDV™ Technologies, the leader in Design and Verification Intellectual Property (IP), today unveiled a tool suite that automates the protocol debugging process and testbench creation by eliminating tedious and error-prone manual approaches and improving productivity.

The automation suite includes SmartViP Debug™, a tool that automatically identifies protocol violations with visual and tabular views, and SmartTestBench™. SmartTestBench automates the creation of testbench files, either through a graphical user interface or through text files, and supports a wide variety of verification scenarios.

“Detecting, debugging and fixing protocol violations is a critical part of the verification flow,” says Deepak Kumar Tala, SmartDV’s managing director. “It is also time-consuming and typically requires detailed knowledge about the specific protocol

being debugged. Developing testbenches manually is tedious work and often leads to errors. That's why customers will find SmartDV's automation tool suite a welcome addition to our product portfolio."

SmartViP Debug works with all industry-standard waveform viewers and uses a profile-based architecture that supports all industry-standard protocols. Its visual and tabular views highlight protocol violations in waveform view while displaying a waveform showing the proper protocol behavior for rapid troubleshooting without requiring the user to be a protocol expert. It supports multiple verification environments including simulation, emulation and SystemC.

SmartTestBench automates the creation of testbench files to support a wide variety of verification scenarios. Those scenarios include: SystemC and transaction-level modeling (TLM); Verification IP in UVM, OVM; SystemVerilog and SystemC; Assertion IP for use in Formal Property Verification; SimXL™, Synthesizable transactor-based acceleration for emulators and FPGA prototype; and post-silicon verification.

It automates the process of testbench creation through an intuitive graphical user interface (GUI) allowing the user to visually add protocols, select protocols and type of IP, and configure the testbench for each protocol and IP type.

SmartTestBench also supports the testbench creation process via text file input and connects directly to SmartViP Debug to provide visual debugging during the testbench creation process, a faster and more efficient approach than manually searching through testbench files. It is fully customizable to fit the user's design configuration requirements to accelerate the testbench creation process and create higher quality testbenches.

Availability and Pricing

The automation suite is available now and provided as a no-cost, value-added complement to SmartDV Verification IP customers.

Email requests for datasheets or more information should be sent to sales@Smart-DV.com.

About SmartDV

SmartDV™ Technologies offers the largest portfolio of Design and Verification Intellectual Property (IP) used by more than 200 customers worldwide, including seven of the top 10 semiconductor companies and four of the largest consumer electronics companies. It supports market segments and protocols as diverse as mobile and 5G, networking and SoC, automotive and serial bus, storage, video and defense and aerospace. With more than 600 products in its portfolio, SmartDV covers the design flow with Design IP and Verification IP for use in simulation, emulation, formal and post-silicon validation and memory models. With the best customer service from more than 250 experienced ASIC and SoC design and verification engineers, a global footprint and local sales offices, SmartDV's technical support is available 24 hours a day seven days a week. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

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